REMARKS

Claims 2-12, and 18-23 are pending in the present application. Claims 2-12 have been amended. Claims 18-23 have been presented herewith. Claims 1 and 13-17 have been canceled.

Priority Under 35 U.S.C. 119

Applicants note the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Information Disclosure Statement

An Information Disclosure Statement has been filed concurrently herewith. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement, and to confirm on the record that the corresponding documents will be considered and cited of record in the present application**.

Claim Rejections-35 U.S.C. 112

Claims 1, 2 and 13 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claims 1 and 13 have been canceled. Claim 2 has been amended to feature that "the data is being transmitted to the host". Applicants respectfully submit that the claims are in compliance with 35 U.S.C. 112, second paragraph, and thus respectfully urge the Examiner to withdraw this objection.

Claim Rejections-35 U.S.C. 102

Claims 1-8 and 13-17 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Moore et al. reference (U.S. Patent No. 6,378,011), This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The Moore et al. reference intends, according to column 3, lines 33-43, to provide a hardware assisted digital phone interface for use in functioning with Advanced Mobile Phone Service (AMPS) cellular phones, which are operable with very little overhead to its digital signal processor (DSP). The Moore et al. reference also aims at improving the synchronous parallel to asynchronous serial throughput rate and overall DSP Input/Output efficiency through the implementation of specialized buffering registers that allow the interface to optimize the buffer threshold and fill levels based upon the protocol specifications provided to the interface by the DSP.

According to column 3, lines 63 through to column 4, lines 24 of the Moore et al. reference, the serial data module contains three main submodules designed to assist the DSP with serial data operations: an asynchronous serial data (ASD) module, a hardware timer and an EEPROM control module. The bus controller includes an independent ASD Tx control module and an ASD Rx control module.

As described in column 7, lines 39-42 of the Moore et al. reference: "[P]roper utilization of these registers allows the DSP to specialize the number of bytes sent together and to optimize the size based on the selected protocol." As further described

in column 7, lines 43-50 of the Moore et al. reference: "[A]nother useful register combination are the ATFFL 151 and ARFFL registers. Using these registers, the DSP can determine the number of reads or writes necessary to empty or fill the FIFO. This means the DSP can avoid polling the FIFO full button each time it attempts to transmit values. A further advantage of the preferred embodiment is that some of the interrupts can be controlled by the SDCR 111."

In addition, as described in column 7, line 60 through to column 8, line 21 of the Moore et al. reference with respect to Fig. 2, the operation of the serial data module includes receiving and disassembling asynchronous data. The operation of the serial data module in transmitting and assembling asynchronous data is described in column 8, lines 37-61 of the Moore et al. reference, with respect to FIG. 5. Specifically, described are the setting of a transfer enable bit and the detection of a start bit, the satisfaction of a query condition, the detection of a last bit, positive for reception and negative for transmission, and the loading procedure in reception.

Applicants respectfully submit that these teachings reveal that the Moore et al. reference merely provides a hardware assisted DSP interface adapted to monitor the transmission and reception registers, to establish control so as to avoid data from overlapping.

In contrast, in the communication terminal of claim 18, the transmission buffer circuit functions responsive to a first write pointer and a first read pointer, and the reception buffer circuit functions responsive to a second write pointer and a second

read pointer. This permits transmission and reception to be controlled separately from and simultaneously with each other.

More specifically, for example, the first write and read pointers are used to provide internal interruption prior to the transmission buffer circuit becoming empty of data. This adjusts the period of time from the occurrence of the internal interruption to the point at which the transmission buffer circuit has the data written thereto, during which such period nothing would otherwise be transmitted, thus maintaining continuous writing and reading of data. In connection with the internal interruption, the buffer controller provides the transmission buffer circuit with a difference of the entire data capacity from a predetermined amount, in order to prevent the transmission buffer circuit from overflowing when transmitting data. This minimizes an overhead time inherent to the interruption, increasing efficiency during data transmission. This is also the case with the reception buffer circuit.

Applicants respectfully submit that the Moore et al. reference fails to teach or even suggest first and second read pointers, and first and second write pointers as featured in claim 18, and fails to minimize the period of time in which nothing is transmitted. The Moore et al. reference thus cannot provide the advantages of transmitting and receiving data in a single cycle and of high-speed asynchronous transmission as realized by the communication terminal of claim 18. Applicants therefore respectfully submit that the communication terminal of claim 18 distinguishes over the Moore et al. reference as relied upon by the Examiner, and that this rejection,

insofar as it may pertain to claims 2-8 and 18, is improper for at least these reasons.

Applicants also respectfully submit that the method of transmitting data of claim 19 distinguishes over the Moore et al. reference as relied upon by the Examiner for at least somewhat similar reasons as set forth above. The Moore et al. reference as relied upon by the Examiner does not disclose "providing the transmission buffer circuit with a first write pointer designating an address location which the data is to temporarily be written into and a first read pointer designating an address location where the data is temporarily stored..."; and "providing the reception buffer circuit with a second write pointer designating an address location which the data is to temporarily be written into and a second read pointer designating an address location where the data is temporarily stored...", whereby transmission and reception of the data are performed simultaneously and separately from each other. Applicants therefore respectfully submit that this rejection, insofar as it may pertain to claims 19-22, is improper for at least these reasons.

The communication terminal of claim 23 includes in combination a transmit data memory that respectively stores and reads data responsive to a first write pointer and a first read pointer, and a receive data memory that respectively stores and reads data responsive to a second write pointer and a second read pointer. The Moore et al. reference as relied upon by the Examiner does not appear to disclose these features. Applicants therefore respectfully submit that the communication terminal of claim 23 distinguishes over the Moore et al. reference as relied upon by the Examiner, and that

this rejection, insofar as it may pertain to claim 23, is improper for at least these reasons.

Claim Rejections-35 U.S.C. 103

Claims 9-12 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Moore et al. reference, in view of well known radio communication standards as evidenced by the Bridgelall reference (U.S. Patent No. 6,717,516). Applicants respectfully submit that the Bridgelall reference as secondarily relied upon by the Examiner does not overcome the above noted deficiencies of the Moore et al. reference, and that this rejection is therefore improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

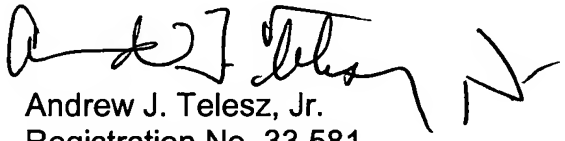
Pursuant to the provisions of 37 C.F.R. 1.17 and 1.126(1), the Applicants hereby petition for an extension of two (2) months to October 18, 2004, for the period in which to file a response to the outstanding Office Action. The required fee of $430.00 should

be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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